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The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. – 10. (Cancelled)

11. (Currently Amended) The resistive memory device of claim 5,

A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface,

wherein the at least one treatment is an exposure to a gas,

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wherein [[:]] the exposure to the gas causes a chemical reaction in the multi-resistive state material and

whereby the properties of the at least one interface are changed by the at least one treatment .

12. - 18. (Cancelled)

19. (Currently Amended) The resistive memory device of claim 1,

A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface,
the bottom surface of the multi-resistive state element arranged on top of and in
direct physical contact with the top surface of the conductive bottom electrode,
the multi-resistive state element having a substantially crystalline layer that, while
substantially maintaining its substantially crystalline structure, has a modifiable
resistance;

a conductive top electrode having a bottom surface and arranged on top of
and in direct physical contact with the top surface of the multi-resistive state
element, wherein the resistance of the resistive memory device may be changed
by applying a first voltage having a first polarity across the conductive electrodes
and reversibly changed by applying a second voltage having a second polarity
across the conductive electrodes;

a top interface created by the direct physical contact between the bottom
surface of the top electrode and the top surface of the multi-resistive state
element; and

a bottom interface created by the direct physical contact between the top
surface of the bottom electrode and the bottom surface of the multi-resistive state
element, at least one of the top interface or the bottom interface includes at least
one treatment primarily directed towards changing properties of the at least one
interface.

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wherein [[:]] the at least one treatment is caused by a chemical reaction between one of the conductive electrodes and the multi-resistive state element, and
whereby the properties of the at least one interface are changed by the at least one treatment.

20. (Previously Presented) The resistive memory device of Claim 19, wherein: an anneal process is a catalyst for the chemical reaction.

21. (Previously Presented) The resistive memory device of Claim 19, wherein: an exposure to a gas is a catalyst for the chemical reaction.

22. - 25. (Cancelled)

26. (Currently Amended) ~~The resistive memory device of claim 1, wherein: the at least one treatment is caused by a bombardment by inert ions.~~

A resistive memory device comprising:

a conductive bottom electrode having a top surface;
a multi-resistive state element having a top surface and a bottom surface,
the bottom surface of the multi-resistive state element arranged on top of and in
direct physical contact with the top surface of the conductive bottom electrode,
the multi-resistive state element having a substantially crystalline layer that, while
substantially maintaining its substantially crystalline structure, has a modifiable
resistance;

a conductive top electrode having a bottom surface and arranged on top of
and in direct physical contact with the top surface of the multi-resistive state
element, wherein the resistance of the resistive memory device may be changed
by applying a first voltage having a first polarity across the conductive electrodes
and reversibly changed by applying a second voltage having a second polarity
across the conductive electrodes;

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a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface.

wherein [[1]] the at least one treatment is caused by a bombardment by inert ions and

whereby the properties of the at least one interface are changed by the at least one treatment.

27. – 28. (Cancelled)

29. (Currently Amended) The resistive memory device of Claim [[28]] 11, wherein:

the at least one layer that is fabricated to be substantially crystalline layer is fabricated to be polycrystalline.

30. (Currently Amended) The resistive memory device of Claim [[28]] 11, wherein:

the at least one layer that is fabricated to be substantially crystalline layer is fabricated to be a perovskite.

31. (Previously Presented) The resistive memory device of Claim 30, wherein:

the at least one interface that is subjected to the treatment is directed towards changing properties of the perovskite.